CLAIMS

1.   A sample and packet synchronization subsystem
interfaced between a cable modem system and a plurality of bit-
rate sampled data transmission devices, the sample and packet
5   synchronization subsystem comprising:

a transmit analog-to-digital / receive digital-to-analog
converter sub-system, including respective buffers for storing
digital sampled data, the respective buffers being coupled
10   between a multiplexer/demultiplexer and respective standard code
/ decode and subscriber loop interface circuits, each standard
code / decode and subscriber loop interface circuit being coupled
to a respective bit-rate sampled data transmission device; and

15   a digital signal processing subsystem, interfaced between
the cable modem system and the transmit analog-to-digital /
receive digital-to-analog converter sub-system, for transmission
and reception through the cable modem system to and from a packet
recipient, the digital signal processing subsystem:
20   determining unsolicited cable modem system grant
arrivals in response to a request from the bit-rate sample data
transmission device;
synchronizing the storing of sampled packets with the
unsolicited cable modem system grant arrivals; and
25   transmitting to the cable modem system upon receipt of
an unsolicited cable modem system grant arrival, currently stored
sampled packets for further transmission to the packet recipient
over the cable modem system.

30   2.   The sample and packet synchronization subsystem of
Claim 1, wherein the digital signal processing subsystem:
for transmission: compresses, packetizes and transmits
compressed signals to the cable modem system, and

for reception: receives incoming digital signals from the cable modem system, depacketizes and decompresses the digital signals and provides decompressed digital signals to the transmit analog-to-digital and receive digital-to-analog converter sub-
5   system.

3.   The sample and packet synchronization subsystem of Claim 1, wherein the digital signal processing subsystem further comprises grant time calculation circuitry coupled between the
10   transmit analog-to-digital / receive digital-to-analog converter sub-system and the cable modem system, the grant time calculation circuitry deriving a clock for standard code / decode and subscriber loop interface circuits based upon clocks of the cable modem system and providing a pointer to indicate a cutoff portion
15   of buffers in which sampled data is being collected to ensure that data collection deadlines are met.

4.   The sample and packet synchronization subsystem of Claim 2, wherein the bit-rate sampled data transmission devices
20   comprises voice packet senders and sampled voice packets from voice packet senders are voice compressed.

5.   The sample and packet synchronization subsystem of claim 1, wherein the packet recipient comprises a Public Switched
25   Telephone Network.